netlist based upon information received from said user interface module and said expert system module; and

a verification module for generating a test bench and a logical verification environment automatically including simulation models based upon information interpreted by said parameter application module.

2. *(Amended)* The System on a Chip (SoC)_netlist builder and verification computer system of Claim 1 wherein said parameter application module creates directions passed to other modules for execution.

A1 (cont'd)

3 *(Amended)* The System on a Chip (SoC) netlist builder and verification computer system of Claim 2 wherein said directions passed to other modules for execution includes command lines.

4 *(Amended)* The System on a Chip (SoC)_netlist builder and verification computer system of Claim 1 wherein said SoC building and verification data provided by said expert system is retrieved from a storage medium comprising a database of building block circuit description files.

5. *(Amended)* The System on a Chip (SoC) netlist builder and verification computer system of Claim 1 wherein said chip level netlist generation module includes the instantiation of internal integrated circuit (IC) devices and connections between the IC devices for internal signals.

6. *(Amended)* The System on a Chip (SoC) netlist builder and verification computer system of Claim 1 wherein said user interface module generates user friendly graphical user interfaces (GUIs) to facilitate selection of standardized circuit blocks and parameterization of the selected standardized circuit blocks.

7. *(Cancelled)*

A2

8. *(Amended)* The system on a chip netlist builder and verification computer method of

Claim 9 further comprising the steps of:

assisting easy entry and modification of user selections and parameters;

presenting information regarding operations of said SoC netlist builder and verification method to a user; and

facilitating selection of standardized circuit blocks and parameterization of said selected standardized circuit blocks.

9. *(Amended)* In a computer system, a system on a chip netlist builder and verification computer method for facilitating creation and modification of internal integrated circuit (IC) designs utilizing existing circuit block designs, said method comprising the steps of:

providing a user friendly interface;

performing a parameter application process;

executing an expert system process;

implementing a chip level netlist generation process including core netlist and 1/0 pin netlists;

verifying a system on a chip design automatically;

creating an underlying structure list;

interpreting information and commands entered by a user; and

performing iterations required to generate an underlying structure list.

10. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

determining which circuit block is selected by a user;

initializing a parameterizable command line string;

processing operations for a circuit block a user has requested;

making an instance specific copy of the parameterizable command line string; and

updating a copy of the parameterizable command line string with user indicated parameters received for a particular instance.

11. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

appending [the] circuit block attributes to other files; and

adding the gate count of a circuit block to a list of gate counts for an IC.

12. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

generating an internal integration list associated with the circuit block **designs**; and

utilizing said internal integration list in the processing of other routines included in an SoC netlist building and verification method.

13. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the step of extracting circuit block descriptions from a storage location based upon [the] applied parameter information.

(cont'd)

14. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

creating an internal integrated circuit (IC) core level netlist in a desired location based on data

structures that were populated in other routines of said SoC netlist builder and verification computer method; and

generating hardware description language VHDL or Verilog code that automatically performs the task of coupling circuit blocks together .

15. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

providing signal declarations;

producing required HDL assign statements in accordance with an assignment list; and

generating the HDL code that will instantiate the signal declarations and HDL assign statements based upon an instantiation list.

16. *(Amended)* [An] A system on a chip netlist builder and verification computer method comprising the steps of: